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Reply to Office Action of 10/21/2004

IN THE CLAIMS

Please amend claims 1, 4-5, 14-15, 25-26, 39-40, 60, 63,
and 69 as follows below.

Please add new claim 70 as follows below.

1 1. (Currently Amended) A method of routing an
2 integrated circuit (IC) design, comprising:
3 accessing the IC design including a plurality of
4 objects on one or more layers;
5 forming a plurality of levels, wherein the plurality of
6 levels includes
7 a first level representing the IC design at a
8 first grid density,
9 a second level representing the IC design at a
10 second grid density finer than at least the first grid
11 density, and
12 a third level representing the IC design at a
13 third grid density finer than at least the first grid
14 density and the second grid density;
15 based at least partly on the IC design, populating each
16 level of the plurality of levels with the plurality of
17 objects; and
18 interconnecting the plurality of objects at one or more
19 of the first level, the second level, and the third level.

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1 2. (Original) The method of claim 1, wherein
2 the routing is multithreaded at least at a first time.

1 3. (Original) The method of claim 1, wherein
2 the routing is single threaded at least at a first
3 time.

1 4. (Currently Amended) The method of claim 1, wherein
2 each of ~~the IC design~~, the first level, the second
3 level, and the third level ~~include~~ includes at least two
4 layers.

1 5. (Currently Amended) The method of claim 1, wherein
2 each of ~~the IC design~~, the first level, the second
3 level, and the third level ~~include~~ includes one layer.

1 6. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 accessing the IC design including a plurality of
4 objects on one or more layers;
5 accessing a first level for the IC design, wherein the
6 first level of the IC design is partitioned into a first
7 plurality of one or more partitions, and the plurality of

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8 objects of the IC design are among the first plurality of
9 one or more partitions; and
10 forming a second level for the IC design, including:
11 partitioning the second level into a second
12 plurality of partitions, wherein one or more partitions
13 of the first plurality of partitions is represented by
14 at least two partitions of the second plurality of
15 partitions; and
16 within each partition of the second plurality of
17 partitions, interconnecting objects substantially
18 independently of other partitions of the second
19 plurality of partitions.

1 7. (Original) The method of claim 6, wherein
2 the routing is multithreaded at least at a first time.

1 8. (Original) The method of claim 6, wherein
2 the routing is single threaded at least at a first
3 time.

1 9. (Original) The method of claim 6, wherein
2 one or more partitions of the first plurality of one or
3 more partitions has no objects of the plurality of objects.

1 10. (Original) The method of claim 6, wherein

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2 every partition of the first plurality of one or more
3 partitions has one or more objects of the plurality of
4 objects.

1 11. (Original) The method of claim 6, wherein
2 interconnecting objects substantially independently is
3 subject at least to boundary conditions of the second
4 plurality of partitions.

1 12. (Original) The method of claim 6, wherein
2 interconnecting objects substantially independently is
3 subject at least to a first partition of the second
4 plurality of partitions locking at least a net shared by at
5 least the first partition and a second partition of the
6 second plurality of partitions to prevent a change of the
7 net by the second partition of the second plurality of
8 partitions.

1 13. (Original) The method of claim 6, wherein
2 each partition of the first plurality of partitions is
3 represented by at least two partitions of the second
4 plurality of partitions.

1 14. (Currently Amended) The method of claim 6, wherein

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2 each of ~~the IC design~~, the first level, and the second
3 level ~~include~~ includes at least two layers.

1 15. (Currently Amended) The method of claim 6, wherein
2 each of ~~the IC design~~, the first level, and the second
3 level ~~include~~ includes one layer.

1 16. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 accessing the IC design including a plurality of
4 objects on one or more layers;
5 accessing a first level for the IC design, wherein the
6 first level of the IC design is partitioned into a first
7 plurality of one or more partitions, and the plurality of
8 objects of the IC design are among the first plurality of
9 one or more partitions; and
10 forming a second level for the IC design, including:
11 partitioning the second level into a second
12 plurality of partitions, wherein one or more partitions
13 of the first plurality of partitions is represented by
14 at least two partitions of the second plurality of
15 partitions;
16 allotting the second plurality of partitions among
17 a plurality of areas, such that each area of the

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18 plurality of areas includes one or more partitions of
19 the second plurality of partitions; and
20 within each area of the plurality of areas,
21 interconnecting objects substantially independently of
22 other areas of the plurality of areas.

1 17. (Original) The method of claim 16, wherein
2 the routing is multithreaded at least at a first time.

1 18. (Original) The method of claim 16, wherein
2 the routing is single threaded at least at a first
3 time.

1 19. (Original) The method of claim 16, wherein
2 one or more partitions of the first plurality of one or
3 more partitions has no objects of the plurality of objects.

1 20. (Original) The method of claim 16, wherein
2 every partition of the first plurality of one or more
3 partitions has one or more objects of the plurality of
4 objects.

1 21. (Original) The method of claim 16, wherein

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2 interconnecting objects substantially independently is
3 subject at least to boundary conditions of the second
4 plurality of partitions.

1 22. (Original) The method of claim 16, wherein
2 interconnecting objects substantially independently is
3 subject at least to boundary conditions of the plurality of
4 areas.

1 23. (Original) The method of claim 16, wherein
2 interconnecting objects substantially independently is
3 subject at least to a first partition of the second
4 plurality of partitions locking at least a net shared by at
5 least the first partition and a second partition of the
6 second plurality of partitions to prevent a change of the
7 net by the second partition of the second plurality of
8 partitions.

1 24. (Original) The method of claim 16, wherein
2 interconnecting objects substantially independently is
3 subject at least to a first area of the plurality of areas
4 locking at least a net shared by at least the first area and
5 a second area of the plurality of areas to prevent a change
6 of the net by the second area of the plurality of areas.

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1 25. (Currently Amended) The method of claim 16,
2 wherein
3 each of ~~the IC design~~, the first level, and the second
4 level, ~~and the third level include~~ includes at least two
5 layers.

1 26. (Currently Amended) The method of claim 16,
2 wherein
3 each of ~~the IC design~~, the first level, and the second
4 level, ~~and the third level include~~ includes one layer.

1 27. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 accessing the IC design including a plurality of
4 blockages and a plurality of pins;
5 forming a graph including a first plurality of nodes,
6 wherein
7 each node of the first plurality of nodes is
8 formed outside every blockage of the plurality of
9 blockages; and
10 interconnecting the plurality of pins through nodes of
11 the graph.

1 28. (Original) The method of claim 27, wherein

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2 the routing is multithreaded at least at a first time.

1 29. (Original) The method of claim 27, wherein
2 the routing is single threaded at least at a first
3 time.

1 30. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 forming a first plurality of nodes for positioning
4 objects of the IC design in a first layer, wherein
5 at least two nodes of the first plurality of nodes
6 are spaced apart by a first interval; and
7 forming a second plurality of nodes for positioning
8 objects of the IC design in a second layer, wherein
9 at least two nodes of the second plurality of
10 nodes are spaced apart by the first interval, and
11 at least two nodes of the second plurality of
12 nodes are spaced apart by one or more intervals greater
13 than the first interval.

1 31. (Original) The method of claim 30, wherein
2 the routing is multithreaded at least at a first time.

1 32. (Original) The method of claim 30, wherein

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2 the routing is single threaded at least at a first
3 time.

1 33. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 forming a first plurality of nodes for positioning
4 objects of the IC design in a first layer, wherein
5 at least two nodes of the first plurality of nodes
6 are spaced apart by a first interval; and
7 forming a second plurality of nodes for positioning
8 objects of the IC design in a second layer, wherein
9 at least two nodes of the second plurality of
10 nodes are spaced apart by the first interval, and
11 at least two nodes of the second plurality of
12 nodes are spaced apart by one or more intervals less
13 than the first interval.

1 34. (Original) The method of claim 33, wherein
2 the routing is multithreaded at least at a first time.

1 35. (Original) The method of claim 33, wherein
2 the routing is single threaded at least at a first
3 time.

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1 36. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 forming a first plurality of nodes for positioning
4 objects of the IC design in a first layer, wherein
5 the first plurality of nodes includes a first
6 plurality of common nodes and a first plurality of
7 uncommon nodes; and
8 forming a second plurality of nodes for positioning
9 objects of the IC design in a second layer, wherein
10 the second layer is at least substantially
11 parallel to the first layer and
12 the second layer is spaced apart from the first
13 layer by about a layer distance along a layer axis,
14 and wherein
15 the second plurality of nodes includes a second
16 plurality of common nodes,
17 the first plurality of common nodes and the second
18 plurality of common nodes share positions, such that if
19 the second plurality of common nodes were shifted
20 toward the first plurality of common nodes by about the
21 layer distance along the layer axis, the first
22 plurality of common nodes and the second plurality of
23 common nodes would be substantially identical,

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24 and wherein if the second plurality of common
25 nodes were shifted toward the first plurality of
26 uncommon nodes by about the layer distance along the
27 layer axis, no node of the first plurality of uncommon
28 nodes and no node of the second plurality of common
29 nodes would be substantially identical.

1 37. (Original) The method of claim 36, wherein
2 the routing is multithreaded at least at a first time.

1 38. (Original) The method of claim 36, wherein
2 the routing is single threaded at least at a first
3 time.

1 39. (Currently Amended) The method of claim 36,
2 wherein
3 each of ~~the IC design~~, the first level, and the second
4 level ~~include~~ includes at least two layers.

1 40. (Currently Amended) The method of claim 36,
2 wherein
3 each of ~~the IC design~~, the first level, and the second
4 level ~~include~~ includes one layer.

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- 1 41. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 defining a volume of the IC design, wherein
4 a subset of the volume carries wiring; and
5 forming a plurality of nodes in the volume, wherein
6 nodes of the plurality of nodes are limited to
7 being formed within the subset of the volume.
- 1 42. (Original) The method of claim 41, wherein
2 the routing is multithreaded at least at a first time.
- 1 43. (Original) The method of claim 41, wherein
2 the routing is single threaded at least at a first
3 time.
- 1 44. (Original) The method of claim 41, wherein
2 the volume includes one layer.
- 1 45. (Original) The method of claim 41, wherein
2 the volume includes at least two layers.
- 1 46. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:

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3 accessing one or more routing pitches of one or more
4 layers of the IC design;
5 defining a volume of the IC design, wherein
6 a subset of the volume carries wiring;
7 forming a first plurality of nodes in the volume; and
8 forming a second plurality of one or more nodes outside
9 the volume, wherein
10 at least one node of the second plurality of one
11 or more nodes is formed at a pitch greater than at
12 least one of the one or more routing pitches.

1 47. (Original) The method of claim 46, wherein
2 the routing is multithreaded at least at a first time.

1 48. (Original) The method of claim 46, wherein
2 the routing is single threaded at least at a first
3 time.

1 49. (Original) The method of claim 46, wherein
2 the volume includes one layer.

1 50. (Original) The method of claim 46, wherein
2 the volume includes at least two layers.

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1 51. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 accessing a first cell instance of the IC design;
4 accessing a second cell instance of the IC design
5 adjacent to the first cell instance, wherein
6 the first cell instance and the second cell
7 instance are spaced apart by a channel;
8 forming a first node near a first end of the channel;
9 forming a second node near a second end of the channel;
10 and
11 connecting a wire directly between the first node and
12 the second node.

1 52. (Original) The method of claim 51, wherein
2 the routing is multithreaded at least at a first time.

1 53. (Original) The method of claim 51, wherein
2 the routing is single threaded at least at a first
3 time.

1 54. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 accessing one or more routing pitches of one or more
4 layers of the IC design;

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5 accessing a first cell instance of the integrated
6 circuit design;
7 accessing a second cell instance of the integrated
8 circuit design adjacent to the first cell instance, wherein
9 the first cell instance and the second cell
10 instance are spaced apart by a channel; and
11 forming a plurality of one or more nodes in the
12 channel, wherein
13 the plurality of one or more nodes in the channel
14 has a pitch greater than at least one of the one or
15 more routing pitches.

1 55. (Original) The method of claim 54, wherein
2 the routing is multithreaded at least at a first time.

1 56. (Original) The method of claim 54, wherein
2 the routing is single threaded at least at a first
3 time.

1 57. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 accessing the IC design including a plurality of
4 objects;
5 accessing a plurality of routing algorithms;

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6 interconnecting, with a first plurality of
7 interconnections, one or more of the plurality of objects,
8 at least partly in response to a first combination of one or
9 more routing algorithms of the plurality of routing
10 algorithms;
11 storing the first plurality of interconnections;
12 automatically determining a second combination of one
13 or more routing algorithms;
14 interconnecting, with a second plurality of
15 interconnections, one or more of the plurality of objects,
16 at least partly in response to the second combination of one
17 or more routing algorithms of the plurality of routing
18 algorithms;
19 comparing results of the first plurality of
20 interconnections and the second plurality of
21 interconnections; and
22 if results of the second plurality of interconnections
23 are worse than results of the first plurality of
24 interconnections, restoring the first plurality of
25 interconnections.

1 58. (Original) The method of claim 57, wherein
2 the routing is multithreaded at least at a first time.

1 59. (Original) The method of claim 57, wherein

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2 the routing is single threaded at least at a first
3 time.

1 60. (Currently Amended) A method of routing an
2 integrated circuit (IC) design, comprising:
3 interconnecting at least a first portion of the IC
4 design at a first routing pitch; and
5 if the interconnecting results in one or more design
6 rule violations, routing at least a part of the first
7 portion of the IC design at a second routing pitch [[less]]
8 different than the first routing pitch.

1 61. (Original) The method of claim 60, wherein
2 the routing is multithreaded at least at a first time.

1 62. (Original) The method of claim 60, wherein
2 the routing is single threaded at least at a first
3 time.

1 63. (Currently Amended) The method of claim 60,
2 wherein
3 the part of the first portion of the IC design routed
4 at the second routing pitch [[less]] different than the
5 first routing pitch includes

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6 a part of the IC design causing at least one of
7 the one or more design rule violations.

1 64. (Original) A method of routing an integrated
2 circuit (IC) design, comprising:
3 interconnecting at least a first part of the IC design
4 on at least a first thread; and
5 interconnecting at least a second part of the IC design
6 on at least a second thread.

1 65. (Original) The method of claim 64, wherein
2 the first thread runs on at least a first processor and
3 the second thread runs on at least the first processor.

1 66. (Original) The method of claim 64, wherein
2 the first thread runs on at least a first processor and
3 the second thread runs on at least a second processor.

1 67. (Original) The method of claim 64, wherein
2 at a first time, both the first thread and the second
3 thread run.

1 68. (Original) The method of claim 64, wherein
2 at a first time, at least one of the first thread and
3 the second thread does not run.

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- 1 69. (Currently Amended) The method of claim 64,
2 wherein [[1)]]
3 at a first time, both the first thread and the second
4 thread run, and [[2)]]
5 at a second time, at least one of the first thread and
6 the second thread does not run.
- 1 70. (New) The method of claim 60, wherein
2 the second routing pitch is less than the first routing
3 pitch.